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EXAMINER	
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ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/759,081	Applicant(s) LI, CHOU H.	
	Examiner William Kraig	Art Unit 2815	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 October 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,3,5,6,8,10,15,16,18-20,22-26,28,30-34,36,38,45-50,52-54,56-74 and 76-85*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attachment sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

EUGENE LEE
PRIMARY EXAMINER

Applicant argues that motivation for combining the Fenner and Kellett references, but in arguing this point, only argues in relation to the instant application and Fenner. Any discussion of the motivation for combining references must necessarily include a discussion of the appropriateness of the combination of references, not simply a discussion of one of the references and how it relates to the instant application.
The remainder of the Applicant's arguments are similar and argue only regarding the singular Fenner reference instead of the combination of references, Fenner and Kellett.

Amendments to the Claims

1. (Previously presented) A commercially mass-produced, integrated circuit (IC) comprising:

a solid substrate of one conductivity type;

a solid material pocket of a different conductivity type having a side surface and positioned on a selected top surface of said substrate;

a signal-translating, electronic rectifying barrier located between said solid material pocket and the selected top surface of said substrate; and

a solid state material region adjoining said solid substrate, said electronic rectifying barrier, and the side surface of said solid material pocket;

said solid state material region having a depth accuracy of better than 0.13 microns and

being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said rectifying barrier, without the almost always present thermally and electrically insulating voids and microcracks visible at 1,000 times magnification in interfacial bonding regions between the bonded device components.

2. (Canceled)

3. (Currently amended) A mass-produced integrated circuit as in claim 1 in which a lateral edge of at least one of said solid substrate, said solid material pocket, and said electronic rectifying barrier has a specified lateral dimension ~~having dimensional accuracy~~ of a few hundred atomic layers.

4. (Canceled)

5. (Previously presented) A mass-produced integrated circuit as in claim 1 in which a selected significant portion of a major surface of at least one of said solid material pocket, said selected top surface of said substrate, said solid state material region, and said electronic rectifying barrier gradually changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

6. (Previously Presented) A mass-produced integrated circuit as in claim 1 in which a selected significant portion of at least one of said solid material pocket, said selected top surface of said solid substrate, said solid state material region, and said electronic rectifying barrier montonically changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

7. (Canceled)

8. (Previously Presented) A mass-produced integrated circuit as in claim 1 in which at least a major surface of one of said electronic rectifying barrier and said solid material pocket is curved.

9. (Canceled)

10. (Previously Presented) A mass-produced integrated circuit as in claim 1 in which the side surface of said solid material pocket is curved over a major portion thereof.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Original) A mass-produced integrated circuit as in claim 1 in which at least one of top and bottom major surfaces of said electronic rectifying barrier is curved.

16. (Previously Presented) A mass-produced integrated circuit as in claim 1 in which a selected portion of said electronic rectifying barrier has a vertical thickness which gradually increases with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

17. (Canceled)

18. (Previously Presented) A mass-produced integrated circuit as in claim 1 in which said electronic rectifying barrier is thin and has a laterally-extending dimension of less than one micron.

19. (Previously Presented) A mass-produced integrated circuit as in claim 1 in which:

said solid state material region consists essentially of a solid material selected from the group consisting of oxide, glass, organics, semiconductor, metal, intermetallics, organics, semiconductor, a dielectrics material, intrinsic semiconductor, and an electrically insulating solid;

said electronic rectifying barrier is selected from the group consisting of a PN junction, a heterojunction, a metal-oxide junction, and a Schottky barrier; and

said solid material pocket is of a semiconductor material selected from the group consisting of Ge, Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

20. (Currently amended) A mass-produced, miniaturized semiconductor device comprising:

a first semiconductor material body having a first polarity;

a second semiconductor material body located generally vertically underneath said first semiconductor material body and having a second polarity that is opposite the first polarity;

a signal-translating, electronic rectifying barrier formed between said first and second semiconductor material bodies; and a third solid state material body having an electrical conductivity at least one order of magnitude different from those of said first and second semiconductor material bodies;

said third solid state material body contacting respective portions of each of said first and second semiconductor material bodies and said electronic rectifying barrier, and having two differentially surface-expanded sides that are not parallel to each other to thereby form on the device a terminal portion ~~of no more than~~ a micron in having a thickness ~~in a selected direction~~ and being accurate to ~~within~~ of a few hundred atomic layers.

21. (Canceled)

22. (Previously Presented) A semiconductor device as in claim 20 in which at least one of said first semiconductor material body, said second semiconductor material body, and said third solid state material body is of an intrinsic semiconductor material.

23. (Previously Presented) A semiconductor device as in claim 20 in which said third solid state material body has an as-formed metallurgically graded-seal continuity of a graded-seal type with respect to at least one of said first and second semiconductor material bodies.

24. (Previously Presented) A semiconductor device as in claim 20 in which the terminal portion of said third solid state material body is vertically within less than a distance from a selected point inside said electronic rectifying barrier;

said distance being selected from the group consisting of one micron and 0.1 microns.

25. (Previously Presented) A semiconductor device as in claim 20 in which said third solid state material body has a geometry, position, and orientation relative to said first and second semiconductor material bodies, to allow adequate stress and strain modification on said electronic rectifying barrier thereby improving device performance.

26. (Previously Presented) A semiconductor device as in claim 25 in which said third solid state material body is favorably stressed, and has a blunt and rounded bottom of zero width so that lateral mismatch stresses at the bottom in the zero width direction is also zero, and

in which the rounded bottom of said third solid state material body is located within a specified distance from a designated point inside said electronic rectifying barrier to achieve a beneficial proximity effect;

said specified distance being selected from the group consisting of one micron and 0.1 microns.

27. (Canceled)

28. (Previously Presented) A semiconductor device as in claim 20 in which said third solid state material body is of an electrically insulating material selected from the group consisting of an oxide, a nitride, organics, semiconductor, metal, intermetallics, a dielectric material, intrinsic semiconductor, other insulator, or a mixture thereof.

29. (Canceled)

30. (Previously Presented) A semiconductor device as in claim 20 in which said third solid state material body has a designed, three-dimensionally controlled shape, size, and location accurate to fractional microns.

31. (Previously Presented) A semiconductor device as in claim 20 in which said third solid state material body has a rounded portion forming an inverted arch making the device more mechanically stable and reliable.

32. (Previously Presented) A semiconductor device as in claim 20 in which the terminal portion of said third solid state material body is less than 1 micron wide in a selected direction.

33. (Previously Presented) A semiconductor device as in claim 20 in which said electronic rectifying barrier has a curved major surface.

34. (Previously Presented) A semiconductor device as in claim 20 in which said third solid state material body has a cylindrical surface.

35. (Canceled)

36. (Previously Presented) A semiconductor device as in claim 20 in which said electronic rectifying barrier is stressed to improve a performance of said semiconductor device.

37. (Canceled)

38. (Previously Presented) A semiconductor device as in claim 20 in which:

said third solid state material body consists essentially of a material selected from the group consisting of a solid, an electrically insulating solid, oxide, glass, organics, semiconductor, metal, intermetallics, a dialectical material, intrinsic semiconductor, and a mixture thereof;

said electronic rectifying barrier is selected from the group consisting of a PN junction, PI junction, NI junction, metal-oxide, oxide semiconductor, interfacial rectifying barrier, and heterojunction, and other optoelectromagnetically active signal-translating region, a Schottky barrier; and a mixture thereof;

said first semiconductor material body is of a semiconductor material selected from the group consisting of Ge,

Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

39. (Canceled)

40. (Canceled)

41. (Canceled)

42. (Canceled)

43. (Canceled)

44. (Canceled)

45. (Previously Presented) An integrated circuit as in claim 1 in which said electronic rectifying barrier adjoins both said solid substrate and said solid state material region at a place where a periphery of said electronic rectifying barrier is differentially surface-expanded to passivate the adjoining rectifying barrier and to reduce noise, instability, leakage current, electrical shorts, and failure due to low breakdown voltage.

46. (Previously Presented) An integrated circuit as in claim 1 in which said solid state material region is a vertically elongated region of less than 1 micron in width or size with an accuracy of less than 0.13 microns, and having a bottom of a shape selected from the group consisting of flat, rounded, cylindrical, hemispherical, and conical or V-shaped.

47. (Previously Presented) An integrated circuit as in claim 1 including means for circulating a rapidly moving cooling fluid in a microscopic vicinity of said signal translating, electronic rectifying barrier to achieve surface cooling of said electronic rectifying barrier.

48. (Previously Presented) An integrated circuit as in claim 1 in which said electronic rectifying barrier has a lateral edge, and at least one of said solid material pocket, said rectifying barrier, and said solid state material region has a portion thereof which gradually and continuously changes its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

49. (Previously Presented) An integrated circuit as in claim 1 in which at least one of said solid material pocket, said rectifying barrier, and said solid state material region has a selected portion thereof which gradually and montonically changes its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

50. (Previously Presented) An integrated circuit as in claim 1 in which a selected portion of at least one of a major surface of said solid material pocket, said electronic rectifying barrier, and said solid state material region is curved.

51. (Canceled)

52. (Previously Presented) An integrated circuit as in claim 1 in which said solid state material region is an

elongated deep and narrow, solid state material region; and including:

a second elongated deep and narrow, solid state material region microscopically close to said elongated deep and narrow, solid state material region;

each of said elongated, deep and narrow, solid state material region and said second elongated deep and narrow, solid state material region being within a micron of both said solid substrate and said electronic rectifying barrier;

said second elongated, solid state material region also having a second submicron width or size at a second terminal portion thereof where it is closest to said electronic rectifying barrier; and

both said elongated, solid state material region and said second elongated, solid state material region having aspect ratios exceeding 3, being oriented normally of a common major bottom surface of said solid substrate, and extending downward from a common top surface of said solid material pocket whereby said elongated, solid state material region and said second elongated, solid state material region are parallel to each other.

53. (Previously Presented) A semiconductor device as in claim 52 in which said elongated, solid state material region and said second elongated, solid state material region have different lengths so that these two solid state material regions reach different depths inside said solid substrate.

54. (Previously Presented) A semiconductor device as in claim 52 in which said elongated, solid state material region and said second elongated, solid state material region differ in

electrical conductivity by at least one order of magnitude from that of the material of said semiconductor material pocket.

55. (Canceled)

56. (Previously Presented) An integrated circuit as in claim 1 in which:

material of said solid material pocket and said solid state material region are solids which are 100% dense, substantially chemically pure and uniform, and non-contaminating, and impervious to contaminating gases;

said solid state material region is stressed to favorably affect a device performance, and has a rounded bottom of zero width so that lateral mismatch stresses at the bottom in the zero width direction is also zero,

said electronic rectifying barrier is located within a specified distance, with a fractional micron accuracy, from a designated point inside said electronic rectifying barrier to achieve a beneficial proximity effect; and

said specified distance being selected from the group consisting of one micron and 0.1 microns.

57. (Previously presented) A mass-produced, low-cost miniaturized solid state device comprising:

a first solid state material of a first conductivity type, a second solid state material of a second conductivity type positioned under the first solid state material, the first and second solid state materials having respective adjoining portions;

a signal-translating, rectifying barrier region lying between the respective adjoining portions; and

a device material region starting at least in the first solid state material and extending toward the rectifying barrier region to form a bottom which is within a micron of a selected point inside the rectifying barrier region;

a major portion of a top surface area of device chip being occupied by circuit elements themselves and not by inert or inactive device material regions thereby achieving radically improved, device miniaturization.

58. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the rectifying barrier region is selected form the group consisting of PN junction, metal-semiconductor or Schottky barriers, heterojunction, metal-oxide, other electrically rectifying barriers, and a mixture thereof;

at least one of the first and second solid state materials is selected from the group consisting of Si, Ge, GaAs, GaP, InP, InSb, intrinsic semiconductor, III-V semiconducting compound, II-VI semiconducting compound, and a mixture thereof;

the device material region penetrates through the rectifying barrier region to reach the second solid state material and, in combination with the rectifying barrier region; electrically isolates device components from one another; and

a bottom of the device material region is less than 0.1 microns and close to zero microns below the rectifying barrier region.

59. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the device material region has a bottom which is closer to zero microns than 0.1 microns below the rectifying barrier region.

60. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the device material region is an elongated device material region; is accurate to less than a micron in a dimension selected from the group consisting of shape, size, depth, and chemical composition profiling; and consists essentially of a device material selected from the group consisting essentially of air, a gas, oxide, nitride, glass, organics, semiconductor, metal, intermetallics, dialectical material, other electrically insulating material, and a mixture thereof.

61. (Previously Presented) A mass-produced, solid state device as in claim 60 in which a bottom of the elongated device material region is close to zero microns below the rectifying barrier region.

62. (Previously Presented) A mass-produced, solid state device as in claim 60 in which the elongated, device material region has an intentionally designed and produced rounded bottom having a curved peripheral surface thereat;

the rectifying barrier region adjoining the rounded bottom of the elongated device material region and having a matching curved peripheral surface thereon thereby passivating and differentially expanding greatly the curved peripheral surface of the rectifying barrier region for protection against Type I contaminants, for eliminating wasteful central flat portions at bottoms of similar device material regions in prior art devices, for reducing mismatch thermal stresses leading to electrical device failures, for minimizing electrical field gradient across a surface passivated and expanded, rectifying barrier region, and for improving mechanical and electrical device yields and reliabilities.

63. (Previously Presented) A mass-produced, solid state device as in claim 57 in which only a minor portion of a top surface area of device chip is not occupied by device circuit elements themselves;

said device circuit elements having no centrally large and flat bottoms as in oxidized isolation bottoms of Peltzer and Murphy devices, thereby achieving radically improved device miniaturization.

64. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the first solid state material is purposely broken up into a plurality of smaller material patches so that mismatch stresses from varying coefficients of material thermal expansions are reduced in proportion to the smaller size of the broken material patches thereby improving device performance.

65. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the device material region is an elongated, cylindrical device material groove having both an aspect ratio of over 3 to 5 and a cylindrical radius of less than one micron, and is oriented generally normally of a top surface of the second solid state material.

66. (Previously Presented) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove is purposely tilted relative to atop surface of the second solid state material so that the device material groove is above a bottom plane of the rectifying barrier region at some places where the groove depth is less than zero (or h<0), substantially coincides with the same bottom plane of the

rectifying barrier region at another place where the groove depth is zero (i.e., h = 0), but lies below the same bottom plane of the rectifying barrier region at other places where the growth depth is greater than zero (or h>0).

67. (Previously Presented) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove has a cylindrical radius of less than one micron.

68. (Previously Presented) A mass-produced, solid state device as in claim 65 including at least one additional, elongated, cylindrical device material groove oriented normally of a top surface of the second solid state material, and microscopically close to the other elongated, cylindrical device material groove;

both the two device material grooves having sizes of less than two microns and different lengths to thereby extend vertically downward from a common higher, vertical level to different depths into the second solid state material.

69. (Previously Presented) A mass-produced, solid state device as in claim 65 in which a bottom of the elongated cylindrical device material groove is above the rectifying barrier region so as to have a groove depth of less than 0.1 microns but microscopically close to zero microns and designed specifically for at least one of thermal, magnetic, and electrical contacting or for optical communication to the device, without actual physical exposure to ambient of the second solid state material.

70. (Previously Presented) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove is real-time feed-back controlled to submicron accuracy in a depth to as close to zero microns below the rectifying barrier region as possible, yet still to have a meaningful device yield to be commercially viable because of the submicron depth accuracy.

71. (Previously Presented) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove has a rounded bottom; and

the rectifying barrier region adjoins a rounded bottom of the device material groove at a curved peripheral surface thereof, thereby maximizing the peripheral surface expansion and minimizing electrical field gradient across the rectifying barrier region to improve device yield and manufacturability.

72. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the device material region is an elongated groove having a microscopically precise groove bottom surface suitable for introducing a precise amount and shape of a foreign matter through the newly formed, highly precise groove bottom surface, thereby achieving microscopically precise three-dimensional control as to shape, size, and position of a region of the foreign matter introduction into the device.

73. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the device material region is a vertical and electrically insulating, elongated device material groove; and

a lower end of the vertical, elongated groove has a centrally rounded bottom of substantially zero width in a

direction parallel to a top major surface of the second solid state material whereby mismatch stresses in the direction arising from varying coefficients of thermal expansions of different materials in the device are substantially zero in the direction thereby improving device yield, performance, and reliability.

74. (Previously Presented) A mass-produced, solid state device as in claim 57 in which the rectifying barrier region has a curved peripheral surface to achieve enhanced device reliability; increase yield; decreased cost; improved junction surface passivation; increased packing density; increased switching speed; reduced noise, instability, leakage current and electrical shorts; improved breakdown voltage; controlled carriers generation, movement, and recombination at or near the junction region peripheral surface; and regulated optoelectromagnetic interaction of the rectifying barrier region with ambient or contacting material.

75. Canceled

76. (Previously presented) A commercially mass-produced IC of Claim 1, in which a selected surface of one or said solid substrate, said solid material pocket, and said rectifying barrier contacts a non-flat surface or a number of the rest of said solid substrate, said solid material pocket, and said rectifying barrier; said number being one or two.

77. (Previously presented) A commercially mass-produced IC of claim 76 in which:

said selected surface is selected from the group consisting of a side surface, a top major surface, and a bottom major surface; and

having a shape selected from the group consisting of: (a) a round surface; (b) a major-portion rounded surface; and (3) a surface rounded in its entirety.

78. (Previously presented) A commercially mass-produced IC of claim 1 in which, on a vertical cross-section thereof, two selected points on at least a number of a top major surface of said solid substrate, a top and a bottom major surfaces of said solid material, pocket, a top and a bottom major surfaces of said rectifying barrier, and a bottom major surfaces of said solid state material region are at two different vertical levels;

said number being selected from the group consisting of one, two, three, four, five, and six.

79. (Previously presented) A commercially mass-produced IC of claim 1 in which, on a vertical cross-section thereof, two selected points on at least a number of a top major surface of said solid substrate, a top and a bottom major surfaces of said solid material pocket, a top and a bottom major surfaces of said rectifying barrier, and a bottom major surfaces of said solid state material region are non-flat but curved in a way selected from the group consisting of: (a) a substantial portion thereof curved; (b) a major portion thereof curved; and (3) curved in its entirety.

80. (Previously presented) A commercially mass-produced IC of claim 1 in which, on a vertical cross-section thereof, a specified portion on at least a number of a selected top and a

selected bottom major surfaces of said solid substrate, a selected top and a selected bottom major surfaces of said solid material pocket, and a selected top and a selected bottom major surfaces of said rectifying barrier, and a selected top and a selected bottom major surfaces of said solid state material region are non-parallel to a number of said other selected surfaces except for a selected nearby contacting surface;

said number being selected from the group consisting of one, two, three, four, five, six, and seven.

81. (Previously presented) A commercially mass-produced IC of claim 1 in which said substrate has a first top major surface and a second bottom major surface, and said electronic rectifying barrier has a third top major surface and a fourth bottom major surface;

at least one of said first, second, third, and fourth major surfaces being non-parallel to at least a number of said other three major surfaces;

said number being selected from the group consisting of one, two, and three.

82. (Previously presented) A commercially mass-produced IC of claim 1 in which said rectifying barrier contacting said material region has one of the following shapes: a) at least a selected portion of the contacting rectifying barrier is non-flat; b) at least a selected portion of the contacting rectifying barrier is curved; c) at least a major portion of the contacting rectifying barrier is non-flat; d) at least a major portion of the contacting rectifying barrier is curved; e) said contacting rectifying barrier is non-flat in its entity; f) said contacting rectifying barrier is curved in its entity; g) said contacting rectifying barrier is non-flat substantially in its

entity; and h) said rectifying barrier substantially is curved substantially in its entirety.

83. (Previously presented) A commercially mass-produced IC of claim 1 in which, on a vertical cross-section thereof, selected respective portions of a top major surface of said solid substrate, a bottom major surface of said solid material pocket, and a top major surface of said rectifying barrier are all curved;

at least one of three selected curved portions has a first peripheral surface contacting, at a contact area, a second peripheral surface of another of the three selected curved portions;

said first peripheral surface being differentially surface-expanded at said contact area over an area selected from the group consisting of: (a) a specified portion thereof; (b) a major portion thereof; (c) the entirety thereof; and (d) substantially the entirety thereof.

84. (Previously presented) A commercially mass-produced IC of claim 57 in which said device material region comprises a cooling fluid.

85. (Previously presented) An IC of Claim 1, wherein said solid state material region has a bottom located within a specified vertical distance from a selected point inside said rectifying barrier;

said specified distance being selected from the group consisting of: a) one micron; b) 0.1 microns; c) substantially zero; d) between 0 and 0.1 microns; and e) between 0 and 0.1 microns but closer to 0 microns than to 0.1 microns.

REMARKS

Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 52-54, 56-74, and 76-85 are pending in this case. Claims 2, 4, 7, 9, 11-14, 17, 21, 27, 29, 35, 37, 39-44, 51, 55, and 75 have been canceled. Claims 2 and 20 are amended herein. No new matter has been added.

Double Patenting

The Examiner has provisionally rejected Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 23-26, 26, 30-34, 36, 38, 45, 46,48-50 and 56-61 as unpatentable on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 44-53 of copending U.S. Patent Application No. 08/483,938. Applicant notes that such application issued as U.S. Patent No. 7,038,290 ("the '290 patent") on May 2, 2006 and that the noted claims 44-53 correspond to claims 11-20 in the '290 patent. As such, Applicant will treat this as a nonstatutory obviousness-type double patenting rejection over claim 11-20 in the '290 patent.. This rejection is respectfully traversed.

Present claim 1 is directed to a commercially mass-produced integrated circuit having a solid substrate of one conductivity type; a solid material pocket of a different conductivity type having a side surface and positioned on a selected top surface of the substrate; a signal-translating, electronic rectifying barrier located between the solid material pocket and the selected top surface of the substrate; and a solid state material region adjoining the solid substrate, the electronic rectifying barrier, and the side surface of said solid material pocket; wherein the solid state material region has a depth accuracy of better than 0.13 microns and is continuously and perfectly bonded metallurgically to all of the solid substrate, the solid material pocket, and the rectifying barrier, without

the presence of thermally and electrically insulating voids and microcracks that visible at 1,000 times magnification in interfacial bonding regions between the bonded device components.

Applicant points out that the present invention is directed to commercially mass-produced integrated circuit devices, which are different than, and on orders of magnitude more difficult to manufacture than, the solid state and active semiconductor devices of the '290 patent.

Specification

The Examiner has objected to the specification, alleging that Claim 20 recites "a terminal portion" in line 17, but that there is no antecedent basis for this term in the specification. Applicant respectfully submits that this objection is obviated in view of the amendment to the Specification.

Section 112, Second Paragraph Rejections (Indefiniteness)

The Examiner has rejected claims 3, 5, 20, 22-26, 28, 30-34, 36, 38 and 75 under 35 U.S.C. 112, second paragraph, as indefinite for the reasons set forth in the Office action. In view of the amendments made herein, Applicant respectfully submits that these rejections have been obviated.

Section 103 Rejections

The Examiner has rejected the pending claims under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 4,916,716 ("Fenner") in view of U.S. Patent No. 3,341,754 ("Keller"). This rejection is respectfully traversed.

Applicant respectfully submits that the Examiner has failed to establish a prima facie case of obviousness. As set forth in

MPEP 706.02, in order to establish a prima facie case of obviousness, the Examiner must, among other things, provide an explanation as to why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed invention. In the present case, the Examiner states that such motivation would be due to "meet basic design needs". However, Applicant respectfully submits that this is not accurate.

In this regard, Applicant points out that the device of Fenner is a Fig. 1 device is on a "Varactor Diode", which is an isolated, single unintegrated semiconductor diode device; it is not an integrated circuit as is the present invention. Further, in the present invention, all claims are directed to commercially mass-produced integrated circuits that call for extremely high dimensional precision and quality/yield to be commercially profitable and mass-producible. By contrast, Fenner claims only a single, isolated unintegrated semiconductor diode device having no other similar neighboring devices to isolate from. As such, motivation for combining the Fenner and Keller references cannot be found in simply meeting device design needs, and accordingly Applicant respectfully submits that the Examiner has not established a case of prima facie obviousness

Further, Applicants states that Fenner has a filing date more than eighteen years before the filing date of Applicant's U.S. Patent No. 3,430,109, which clearly discloses the use of oxide isolating grooves of various bottom shapes (see, for example, col. 2, lines 4-6), not just to guard the PN junction but, more importantly, to passivate the PN junction and to electrically isolate neighboring semiconductor devices on the same chip in an integrated circuit. Furthermore, the oxide groove has a cylindrically rounded bottom with zero bottom width

to maximize device miniaturization for oxygen masked diffusion process. The bottom of the oxide groove is down to 0.1 or near zero microns below the PN junction region. Fenner could not reliably and reproducibly mass-produce such devices, at least not in a commercially profitable manner. In order to achieve junction passivation, Applicant's oxide groove provides a rounded PN junction peripheral surface with a very large, surface or differential surface expansion for minimum leakage currents and maximum breakdown voltages. Only automatic groove forming methods with real time feed-back control, as disclosed in Applicant's '109 patent (see, for example, col. 2, lines 38-68), and in other patents, can produce smaller than submicron groove sizes, depths, and locations.

Furthermore, Applicant notes that, in his later U.S. Patent Application No. 154,300, filed June 18, 1971, and U.S. Patent No. 4,946,800, filed August 7, 1973, he disclosed that a rounded groove bottom reduces thermal mismatch stresses, and can, according to mobility tests, modify the stress and strain in silicon to improve device other performances. Applicant's U.S. Patent No. 3,585,714 patent deals in *Figs.* 6-7 hundreds of integrated devices on a single chip. Later patents are for new applications dealing with thousands, millions, and billions of physically integrated circuit devices on a single chip. The many, many components are electrically isolated from one another on a single chip by Applicant's unique oxide isolating grooves. The layer thicknesses, dimensions, radii, positions, depths, and stresses and strains in individual device components are orders of magnitude different from other devices. They are much more difficult to produce than those in Fenner's singular, un-integrated diodes. Applicant's '109 patent, which was filed in 1965, not only clearly discloses but, more importantly, explains in great details the minimum requirements, exact procedures, and

special automation equipment and technique to make the unique oxide-isolating grooves of zero bottom widths enabling highly miniaturized modern electronics

Moreover, Applicant notes that in Fenner (see Figure 1), whether the 4/3 rectifying barrier between layers 4 and 3 is a PN junction or Schottky barrier, the vertically flat or planar, non-curved, and unexpanded (certainly not "differentially surface expanded") junction peripheral surface was met by the equally vertically flat or planar and having non-expanded nor differentially expanded side surface on the pocket 7. Note that the metal or p-conductive layer 4 not only is flat-sided, and totally and irrelevantly above the weakly n-conductive semiconductor layer 3 by approximately 0.1 to 2 microns. See Fenner at col. 2, lines 55-60. The n-conductive semiconductor layer 3 is also flat-sided and totally above the hemi cylindrically "rounded" channel bottom of channel 7. Hence, the PN or Schottky rectifying barrier 4/3 is already over 0.1 and 2 microns above the "curved" portion of the channel bottom 7. The rectifying barrier was guarded but not passivated, and was easily contaminated by metals or dust particles to cause the same worldwide leakage current epidemic resulting in poor device yield and high cost, as explained in '109, at col. 4, line 56 to col. 5, line 41. Further, the flat-sided peripheral surface of the barrier has absolutely no surface expansion or differential surface expansion - another feature of Applicant's unique oxide grooves. Accordingly, the device of Fenner does not have passivated PN Junctions, expanded barrier peripheral surface, nor stress and strain relief for lack of curvature on the peripheral surface, and other features of Applicant's patented devices.

Applicant further notes that there is no other device to isolate from on the same chip. In the Fenner device, whether

the annular channel 7 shape is cylindrical, spherical, paraboroidal, conical, flat, or rounded (See Applicant's '109 patent at col. 2, lines 5-6) had nothing to do with the device breakdown voltage, leakage current, and device yield, and little to do with the overall diode size or miniaturization. Yet device miniaturization is extremely important in modern microelectronics where high miniaturization is absolutely necessary. Without device yield, there would be no products to sell. Without device miniaturization, there is no device miniaturization and, therefore, modern electronics, regardless of what the channel 7 shape, thickness, or location. The dimension of the various diode dimensions, the accuracy of the diode component dimensions, or the bonding qualities between the different diode component materials are then unimportant or irrelevant.

Applicant further notes that the use of intrinsic semiconductor material together with other doped semiconductor materials on the same semiconductor device was first specifically disclosed as Figures 3a and 3b in Applicant's aforementioned 154,30 application, over nine years before Fenner. But the use of intrinsic semiconductors was not claimed until Applicants' U.S. Patent Application Nos. 08/483,937 and 08/483,938, both filed on June 7, 1995, which generally claim the use of silicon on intrinsic silicon were for improving the impact resistance of these mixed intrinsic and doped semiconductor, single-material (e.g., silicon) devices. Still later, when the semiconductor industry was dead stuck at 100 nm devices because the very thin gate layers were always leaky, Applicant found that the new worldwide leakage currents arose from mismatches of thicknesses and thermal expansion coefficients of the gate layer relative to the substrate. The first of several proposed solutions was the use of silicon on

intrinsic semiconductor in "single-material circuits." Intel tried this approach with "intrinsic silicon sitting on top of silicon." The leakage current was drastically reduced by 1,000 times. The 90 nm barrier was broken, so was 65nm and possibly 35 nm. Applicant could not claim this early because the worldwide universal thin gate layer problem did not exist before about 2002.

Accordingly, Applicant respectfully submits that Fenner does not set forth an enabling disclosure of the subject matter claimed in the present application, as supported by Applicant's discussion of the development of the art in this field, specifically with respect to the use of unique materials thicknesses, configurations, and thermal mismatch coefficients, radii of curvature, processing steps, and equipment for making a commercially mass-producible and profitable integrated circuits for the new technologies listed below.

Accordingly, Applicant respectfully submits that the withdrawal of the outstanding rejections under Section 103 is appropriate and is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and an early notice to that effect is respectfully requested.

Please direct any questions concerning this Response to Applicant's undersigned representative, who can be reached directly at (610) 869-6302.

Respectfully submitted,
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